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EXAMINER	
KIM, EDWARD J	
ART UNIT	PAPER NUMBER
2455	

MAIL DATE	DELIVERY MODE
11/17/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/581,862	GEHRING ET AL.	
	Examiner	Art Unit	
	EDWARD J. KIM	2455	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-10* is/are pending in the application.

4a) Of the above claim(s) *7* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, and 8-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed on 06/30/2008.

2. Claims 1-6 and 8-10 are pending in this office action. Claims 1, 8, and 9 have been amended, claim 7 has been cancelled, and claim 10 has been newly added.

Response to Amendment

3. The Examiner withdraws previous Objections to the claims.

4. The Examiner withdraws previous 35 U.S.C. 112 2nd paragraph rejections regarding claims 1 and 9, and concludes that the claim language may be interpreted in multiple ways as explained by the Applicant (refer to the last paragraph of pg.9 in the Amendment filed on 06/30/2008).

5. The Examiner withdraws previous 35 U.S.C. 112 2nd paragraph rejections regarding claims 8 ("primary control task", "subsidiary task", "primary task").

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 8 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is unclear to what the terms, "primary tasks" and "secondary tasks", are referring to, rendering the claims vague and indefinite to what the claimed subject matter is.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-3, and 5, 6, 8, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kayano et al. (US Patent #5,544,054), hereinafter referred to as Kayano, in view of Chavez (US Patent #7,308,499 B2).

Kayano discloses a vehicle multi-processor control system and method with processing load optimization, where the plurality of control processors are connected by LAN, BUS and so on.

Regarding claim 1, Kayano discloses, a method for operating a software module on a processor unit in a controller networked via a data bus in a vehicle (Kayano, Abstract), wherein i) the software module is executable in a plurality of controllers which interchange data via the data bus (Kayano, Abstract, col.1 ln.42-63, col.1 ln.55-56, col.1 ln.61-65) , ii) selection of the controller on which the software module is operated is made based on the available computational capacity of the controllers which are currently in operation (Kayano, Abstract, col.1 ln.42-63, col.1 ln.44-49), and iii) each of the controllers can turn off the software module when a utilization level of its processor is high, and as soon as the software module has been turned off, the software module is to be started again on another controller (Kayano, col.3 ln.45-54, col.11 ln.14-16, col. 7 ln.40-45, col.4 ln.62-67. Software modules are terminated according

to the computing capacity and transferred to run on a different processor.): said method comprising:

a software module, in a controller on which said software module is running, sending to the data bus, either cyclically or upon request, an appropriate identifier containing information indicating the software module's operating status and the identity of the controller on which the software module is running (Kayano, col.1 ln.42-62, col.2 ln.65 – col.3 ln.12, col.3 ln.40-47, col.6 ln.40-47. Kayano discloses a method and system where software modules are transferred to be run on processors with less load or in other words, less utilization rate. The system is disclosed to be constantly acknowledging changes in the load state and adjusts accordingly.);

checking cyclically to determine whether and on which controller the software module is running, based on said identifier (Kayano, col.1 ln.42-62, col.2 ln.65 – col.3 ln.12, col.3 ln.40-47, col.6 ln.40-47.);

wherein said determining step is made by based on information sent by the controllers, in rotation or by means of a request, wherein the information is indicative of their available computational capacity (Kayano, col.1 ln.42-62, col.2 ln.65 – col.3 ln.12, col.3 ln.40-47, col.6 ln.40-47.).

Kayano discloses that the processor with lower load, greater capacity available, is chosen for executing the software (Kayano, col.6 ln.40-49). It was common and well-known in the art of at the time the invention was made to select a processor which has the greatest free computation capacity for executing a software module, as shown by Chavez (Chavez, col.3 ln.4-15. Chavez discloses a method for dynamic load balancing in a network, where the processor with the greatest free computation capacity is chosen.). Processor clock frequencies are

commonly used in the art to distinguish processor types. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Kayano to select the processor with the greatest computation capacity for executing the software module.

Regarding claim 2, Kayano and Chavez disclosed the limitations, as described in claim 1, and further discloses, a method wherein before the software module is executed it is ascertained which of the controllers provides the maximum free computation capacity and the software module is started on the determined controller (Kayano, col.3 ln.45-54, col.11 ln.14-16, col. 7 ln.40-45, col.4 ln.62-67. Software modules are terminated according to the computing capacity and transferred to run on a different processor. Chavez, col.3 ln.4-15. Chavez discloses a method for dynamic load balancing in a network, where the processor with the greatest free computation capacity is chosen.).

Regarding claim 3, Kayano disclosed the limitations, as described in claim 1, and further discloses, a method wherein the controller on which the software module is running compares its computation capacity with the computation capacity of the other controllers and either continues to operate or terminates operation of the software module based on the comparison (Kayano, col.3 ln.45-54, col.11 ln.14-16, col. 7 ln.40-45, col.4 ln.62-67. Software modules are terminated according to the computing capacity and transferred to run on a different processor.).

Regarding claim 5, Kayano and Chavez disclosed the limitations, as described in claim 1, and further discloses, a method wherein the software module is started on a controller having the maximum free computation capacity (Kayano, col.3 ln.45-54, col.11 ln.14-16, col. 7 ln.40-45, col.4 ln.62-67. Software modules are terminated according to the computing capacity and

transferred to run on a different processor. Chavez, col.3 ln.4-15. Chavez discloses a method for dynamic load balancing in a network, where the processor with the greatest free computation capacity is chosen.).

Regarding claim 6, Kayano disclosed the limitations, as described in claim 1, and further discloses, a method wherein the software module is stored in a memory in the controllers (Kayano, col.1 ln.60-63, col.3 ln.51-67).

Regarding claim 8, Kayano discloses, a networked controller having software modules stored in a controller's memory; wherein:

the software modules perform primary tasks; a software module with a secondary task can be additionally stored in a microcontroller's memory by the controllers (Kayano, Abstract, col.1 ln.42-65, col.2 ln.65 – col.3 ln.12, col.3 ln.40-47, col.6 ln.40-47);

the controllers have process cycles; a process cycle is terminated after a particular time has elapsed, the data ascertained in the process are output onto the data bus, and the process cycle is started again; the process cycle for the controllers is determined by the software modules for one of the primary tasks, the operating system and a bus protocol; and when a process cycle or a process cycle time has elapsed, data is sent to the data bus which characterize their current processor utilization level and processor type used, with the controllers using this data to ascertain the utilization level of the other controllers.

In regards to the above limitations set forth by the claim, Kayano discloses a method and system where software modules are transferred to be run on processors with less load or in other words, less utilization rate. The system is disclosed to be constantly and regularly acknowledging changes in the load state and adjusts accordingly (Kayano, col.1 ln.42-62, col.2

ln.65 – col.3 ln.12, col.3 ln.40-47, col.6 ln.40-47.). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have set intervals, such as process cycles to output, check, and determine the status of each controller.

Regarding claim 9, Kayano discloses, a method of operating a network of controllers which are coupled via a data bus, each of which controllers has at least one processor, and has installed thereon the same software module which can be executed by the processor contained in any one of the controllers (Kayano, Abstract, col.1 ln.42-63, col.1 ln.55-56, col.1 ln.61-65), each of said controllers being configured such that it can turn off the software module when a utilization of its processor is high (Kayano, col.3 ln.45-54, col.11 ln.14-16, col. 7 ln.40-45, col.4 ln.62-67, col.6 ln.40-49. Software modules are terminated according to the computing capacity and transferred to run on a different processor.), said method comprising: each controller sending via the data bus, information regarding a current utilization level of its at least one processor (Kayano, col.1 ln.42-62, col.2 ln.65 – col.3 ln.12, col.3 ln.40-47, col.6 ln.40-47.);

whenever said software module is running in a particular one of said controllers, said software module in said particular controller sending via the data bus, an identifier indicating the software module's operating state and identifying the particular controller (Kayano, col.1 ln.42-62, col.2 ln.65 – col.3 ln.12, col.3 ln.40-47, col.6 ln.40-47.);

checking said data bus to determine whether an identifier is present; when no identifier is found in said checking step, determining which of the controllers has the greatest available computation capacity, based on its current utilization level as sent via the data bus (Kayano, col.1 ln.42-62, col.2 ln.65 – col.3 ln.12, col.3 ln.40-47, col.6 ln.40-47. Kayano discloses a method and system where software modules are transferred to be run on processors with less load or in other

words, less utilization rate. The system is disclosed to be constantly acknowledging changes in the load state and adjusts accordingly.);

said controller with said greatest available utilization level starting operation of said software module, and said software module sending to said data bus, an identifier indicating the software module's operating status and the identity of the controller in which the software module is running (Kayano, col.1 ln.42-62, col.2 ln.65 – col.3 ln.12, col.3 ln.40-47, col.6 ln.40-47);

when an identifier is present on the data bus in said checking step, the controller on which said software module is running ascertaining its own processor utilization level and comparing its computation capacity with the available computational capacity of other controllers coupled via the data bus (Kayano, col.1 ln.42-62, col.2 ln.65 – col.3 ln.12, col.3 ln.40-47, col.6 ln.40-47);

when the utilization level of the controller on which the software module is greater than that of one of said other controllers, said controller on which said software module is running ceasing operation of said software module; and said one of said other controllers starting operation of said software module, and said software module sending to said data bus an identifier indicating that it is running and identifying said one controller (Kayano, col.3 ln.45-54, col.11 ln.14-16, col. 7 ln.40-45, col.4 ln.62-67. Software modules are terminated according to the computing capacity and transferred to run on a different processor.).

Kayano discloses that the processor with lower load, greater capacity available, is chosen for executing the software (Kayano, col.6 ln.40-49). It was common and well-known in the art of at the time the invention was made to select a processor which has the greatest free

computation capacity for executing a software module, as shown by Chavez (Chavez, col.3 ln.4-15. Chavez discloses a method for dynamic load balancing in a network, where the processor with the greatest free computation capacity is chosen.). Processor clock frequencies are commonly used in the art to distinguish processor types. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Kayano to select the processor with the greatest computation capacity for executing the software module.

Regarding claim 10, Kayano disclosed the limitations, as described in claim 8, and further discloses, wherein the software module sends via the data bus, an identifier indicating the software module's operating state and identifying the particular controller on which the software module is running (Kayano, col.1 ln.42-62, col.2 ln.65 – col.3 ln.12, col.3 ln.40-47, col.6 ln.40-47).

10. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kayano et al. (US Patent #5,544,054), hereinafter referred to as Kayano, in view of Chavez (US Patent #7,308,499 B2), in further view of Official Notice taken by the Examiner.

Regarding claim 4, Kayano disclosed the limitations, as described in claim 1, and further discloses, a method wherein the computation capacity of a controller is ascertained from the processor utilization level and processor type (Kayano, co.1 ln.42-62, col.3 ln.2-4.).

Although Kayano does not explicitly state that the processor type is also considered in the computing the capacity of a controller, "official notice" is taken by the Examiner that this method was well-known in the art at the time the invention was made. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the

teachings of Kayano to take into account the processor type for computing the capacity of a processor. One would have been motivated to do so since it was well-known and common in the art that processor type also determines the computing capacity.

Response to Arguments

11. Applicant's arguments filed 06/30/2008 have been fully considered but they are not persuasive.

12. The Examiner has previously state in the Conclusion section of the previous Office Action,

> **"Examiner's Note:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner." (refer to Office Action – Non-Final Rejection dated 04/04/2008).

13. The Applicant argues,

> "Kayano does not, however, disclose or suggest a software module sending an identifier "containing information indicating the software module's operating status and the identity of the controller on which the software module is running"." (refer to the last paragraph of pg.10 in the Amendment filed on 06/30/2008)

The Examiner respectfully disagrees.

The software module's operating status is disclosed by Kayano in at least the following sections: col.2 ln.65 - col.3 ln.12, col.3 ln.40-47 (load states, present running states, etc.). The identity of the controller, on which the software module is running on, needs to be communicated within the system to allow load-balancing as disclosed by Kayano. Without the

identity of each controllers, the system will not be able to identify which controllers should execute a certain process according to their capacity. The Applicant has failed to clarify in detail how the cited references are different to that of the claimed subject matter.

The Applicant argues,

> "The combination of Kayano and Chavez does not render claim 8 obvious because the combination does not disclose or suggest that "the process cycle for the controllers is determined by the software modules for one of the primary tasks, the operating system, and a bus protocol".

The Applicant discloses, "the process time required by the software module corresponds to the total time during which the software module used a particular processor, from the time when it was started to the execution of the task" (refer to paragraph [0028] of the publication of the application US Pub.#2007/0174683 A1). The Applicant further discloses that when a process cycle or a process cycle time has elapsed, the controllers 1, 3, 5 send to the data bus 8 data which characterize their current processor utilization level..." (refer to paragraph [0030] of the publication of the application US Pub.#2007/0174683 A1).

It is suggested from the cited references that the *process cycle* is determined by the software module, and corresponds to the total time the processor was used, and is utilized for sending data such as the utilization level, state, etc. Since the software modules, present on the system disclosed by Kayano and Chavez, carries out the tasks, the process cycle is determined by the software module. The Applicant further admits that "Kayano discloses the use of ...a 10 ms interval" (refer to the third paragraph of pg.12 in the Amendment filed 06/30/2008). The Applicant has failed to clarify in detail how the cited references differ from the claimed subject matter.

Also, since Kayano discloses that the system is constantly and regularly acknowledging the load states and the utilization level (Kayano, col.1 ln.42-62, col.2 ln.65 - col.3 ln.12, col.3 ln.4047, col.6 ln.40-47), it would have been obvious to one of ordinary skill in the art at the time the invention was made to have set intervals, such as process cycles to output, check, and determine the status of each controller.

In regards to the argument regarding the Official Notice in the rejection of claim 4 in the previous Office Action (dated 04/04/2008), the Examiner references a new a prior art that supports the allegation that the use of a processor type in computing the capacity of a processor was well-known in the art at the time the invention was made (Downs et al., US Patent #6,112,243). Downs et al. discloses the use of processor type in acknowledging the computing capacity of a processor (Downs et al., col.6 ln.39-45).

Conclusion

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to EDWARD J. KIM whose telephone number is (571)270-3228. The examiner can normally be reached on Monday - Friday 7:30am - 5:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Saleh Najjar can be reached on (571) 272-4006. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Edward J Kim/
Examiner, Art Unit 2455

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